

Reliability Embedded Test Engineering (RETE)

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Abstract

The semiconductor production and testing facilities face a major hurdle in the form of intermittent and latent failures occurring in system-on-chip (SOC) devices. Modern HTOL and Burn-In test systems are utilized to perform standardized reliability screening tests (JESD47, JESD22-A108) to achieve “Zero-Defect” semiconductor production. The test systems generate large volumes of data from multiple sources (ATE, burn-in boards, equipment logs and on chip diagnostics), generally stored in formats such as STDF, CSV, etc. Due to such complex data ingestion and focus on the yield of pass/fail assessments, subtle multi-parametric degradation and failures remains undetected, causing burn-in and HTOL conditions to be unnecessarily stringent.

The Reliability Embedded Test Engineering (RETE) is a project being developed collaboratively by Fraunhofer ENAS & ELES Semiconductor Equipment S.p.A. The project focuses on developing an AI-driven reliability analytics software which is complete integrated with ELES Test-for-Reliability (TfR) framework and ART burn-in test systems. Core elements of this software consist of unified test data format, automated data validation and an analytics toolchain library that combines conventional statistics with specialized machine learning modules for failure prediction and lifetime estimation. The goal is to turn HTOL/ELFR process from a time and resource-intensive screening step into a predictive reliability instrument.

1 Introduction

Major application for SOCs in automotive, data center and industrial fields call for extreme reliable lifetimes and safety requirements to ensure accurate operations.

The ELES ART test equipment facilitates a range of standard qualification test capabilities (HTOL, ELFR, PTC, Burn-In, Test during Burn-In). However, there is an industry-wide gap for a single, uniform data structure platform that combines reliability screening, equipment logs and STDF wafer acceptance test data. Linking of these data files with data from Design-for-Test (DfT) instruments such as ring oscillators, thermal and current sensors, BIST signatures and diagnostic registers will be vital to understand drift/degradation mechanisms and intermittent failures. RETE addresses this gap by providing unified data test format and AI supported tool chain that will aid in design and process improvement.

2 Objectives and Methodology

Unified ETDF based data infrastructure that imports diverse file formats such as STDF, CSV, log files and automatically converts them into ELES Test Data Format (ETDF). ETDF stores all measurements and metadata in a centralized database and performs data validation with accurate traceability using test identification parameters (DUT ID, Lot number, Wafer coordinates, Stress intervals).

Structured and scalable analytics workflow for HTOL and ELFR screening. The workflow includes: automated data cleaning, PAT filtering (SPAT, DPAT, MVPAT), SPC, drift analysis, bin & yield analysis, correlation tools, lifetime modelling (MTTF, FIT) and report generation.

Native AI/ML engine with features including:

- Failure mode classification using multiple parametric drifts supporting Design-for-Reliability (DfR)
- Deep learning models for reliable lifetime estimation, anomaly detection and predictions using drift analysis
- ML-enhanced PAT using historical lots and failure cases

Industrial Validation of RETE approach using ELES ART systems provide major technical benefits such as earlier detection of latent faults with improved accuracy and economic impact through Burn-In test optimization.

3 Technical Implementation and Innovation

Software: RETE is implemented as a client-server model (Flutter frontend, Python backend) offered as a Windows desktop application structured for later transition to scalable SaaS deployment. RETE prototype includes an ETDF parse tool with multi file support, filter engine and interactive plotter including statistical analysis tool widgets. RETE proposes an AI/ML engine based to operate on

clean data and automate outlier analysis with known failure classifications and implements fixed analysis predefined for HTOL and ELFR tests with automated report generator creating JEDEC standard qualification reports.

Hardware: RETE implements DfT/DfR features in the DUT and on the test equipment boards to improve data analysis. These elements include scan chains, embedded thermal and current sensors, RMS detectors, current generators, BIST, ring oscillators and diagnostic registers. These elements are then accessed via the ELES architecture enabling continuous monitoring of aging indicators during the stress test for better data interpretation.

4 Results and Impact

Comprehensive summary of RETE workflow:

- Prototype toolchain availability as a desktop application.
- ETDF Data Handling:
 - Multi File ETDF Import
 - File integrity and consistency checks
 - Data validation and interpretation
- Advanced outlier and failure detection tools
- Visualization engine through interactive plotter
- HTOL/ELFR standard analysis configurations
- Automated reporting

As an initial case study, RETE was applied to an ETDF data file containing burn-in analysis of 288 Accelerometer devices for 24 hours. **2 latent failures** were flagged using conventional analysis and **9 additional outliers** were identified using multi-parametric analysis on the acceleration data.

Key impact findings of RETE:

- Improved correlations and finding between stress conditions, failure mechanisms and equipment data
- Enable optimisation of burn-in and HTOL conditions
- AI/ML derived insights can be reintegrated into design and manufacturing process to eliminate major failure mechanisms

5 Conclusion

RETE establishes the use of advanced analytics and artificial intelligence in testing through the combination of a unified ETDF database, DfT & DfR based telemetry and innovative data acquisition architectures. With the case study of accelerometer devices, RETE was able to identify additional nine outliers using advanced analysis algorithms in addition to the two latent failures identified by conventional methods. Detection and characterization of these outliers supports process optimization which results in improved overall device reliability. Therefore, the approach of RETE intends to evolve standard reliability testing platforms into fast, predictive, “Zero-Defect” test infrastructure for semiconductor devices.

6 Literature

- [1] RETE: Design and Test for Reliability. Data Analysis for Zero Defects. Luca Moriconi, Alessandro Maseri, Giovanni Taormina: ARTs23, 2023.

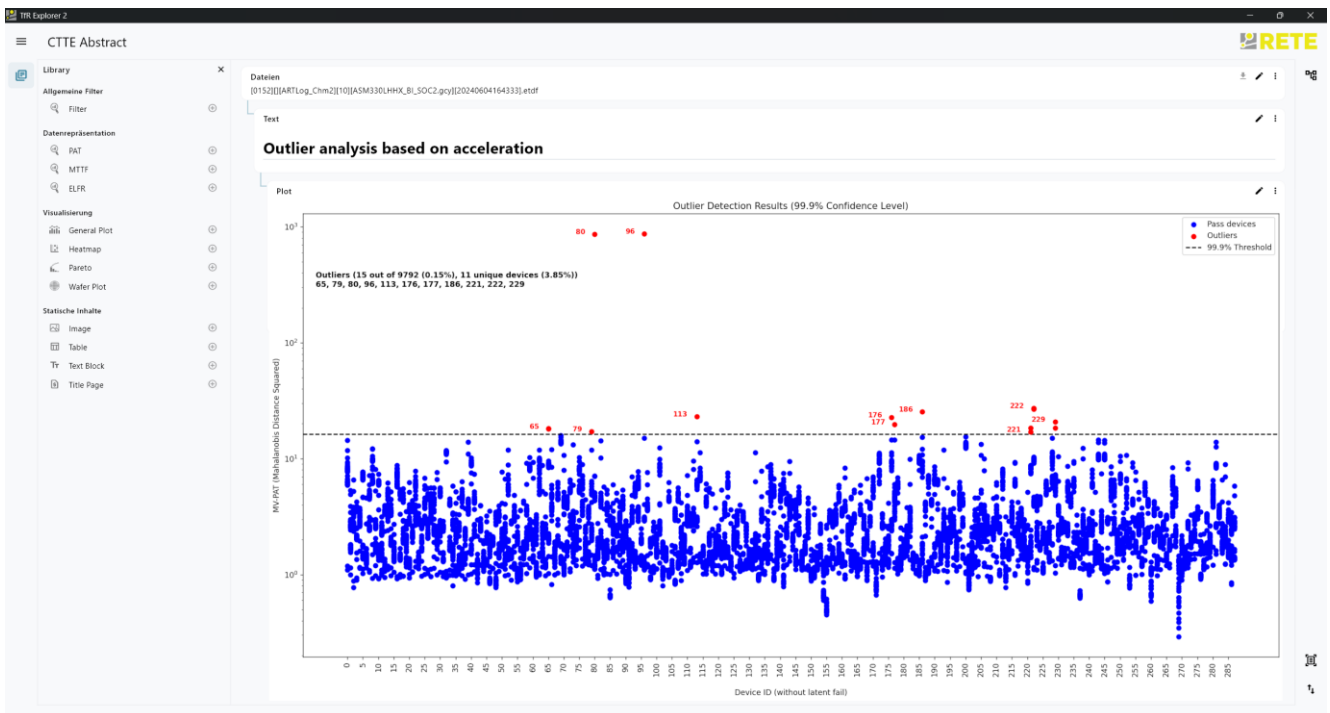


Figure 1: Case Study: Outlier Analysis of 288 Accelerometer devices w.r.t the parameters of acceleration in x, y & z axis.